SIMMWIC Rectennas on High-Resistivity Silicon and CMOS Compatibility

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***Abstract*—Rectifying antennas (rectennas) are realized on high-resistivity silicon substrates using silicon monolithic millimeter-wave integrated circuit (SIMMWIC) technology. Monolithically integrated coplanar Schottky barrier diodes are used as rectifying elements embedded in different antenna structures. Both p- and n-type Schottky barrier diodes are realized with cutoff frequencies up to 1 THz. The rectennas are combined with a CMOS preamplifier mounted as a multichip module (MCM) next to the rectenna on a high-resistivity silicon substrate. An amplification of 32 dB is measured. Maximum sensitivity of the detector circuit including preamplification is 1600 mV/mW $\cdot$ cm^{-2} at 94.6 GHz. For a monolithic integration of high-frequency circuits with low-frequency control and signal-processing electronics, the monolithic integration of CMOS circuitry on high-resistivity silicon is discussed.**

***Index Terms*— CMOS, detector circuits, millimeter-wave circuits, rectenna, Schottky diode, SIMMWIC.**

I. Introduction

ONE OF THE most attractive possibilities of millimeter-wave integrated circuits concerns the monolithic inclusion of planar antennas, which can be diminished to typical Si-chip dimensions (1–10 mm) in the frequency regime above 60 GHz. The technique enabling the monolithic integration of antenna, passive networks, and active devices into microsystems is called silicon monolithic millimeter-wave integrated circuit (SIMMWIC) technology [1] utilizing low-doped (high-resistivity) silicon as the substrate. For an overview, see [1] and [2]. As active devices, two terminal devices will mainly be used because silicon-based IMPATT diodes and Schottky diodes are well established for oscillators and receivers up to 100 GHz and beyond. Recently, Si/SiGe heterobipolar transistors (HBT's) extended their frequency limits to above 100 GHz, establishing them as promising candidates for active devices in microwave circuits. Very recently [4], even CMOS fabrication on float-zone (FZ) high-resistivity silicon was accomplished, opening the route to integrate SIMMWIC's with low-frequency control and signal-processing electronics.

In a future receiver scenario, one could imagine a single-SIMMWIC-chip solution with a switched antenna with variable beam characteristics, a mixer with eventually an external local oscillator (LO), and a preamplifier. In this investigation, we discuss as a subsystem the combination of the antenna with a Schottky diode to a rectifying antenna (rectenna) with and without preamplification. When using a monolithic integrated zero-bias silicon Schottky diode, the rectenna needs no external bias for detection of millimeter-wave radiation.

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II. Rectenna Concept

The rectenna (rectifying antenna) concept basically consists of an antenna and a nonlinear rectifying element where the two elements are merged into a single circuit. Such a module is able to receive and detect microwave power. The frequency selectivity is mainly done by the antenna itself. Since the rectenna is a receiving module collecting power from a radiation field, the sensitivity S_R is characterized by

$$S_R = \frac{\text{output voltage}}{\text{power density at the antenna}}.$$

Division of this value with the effective antenna aperture leads to the normally used quantity for detectors

$$S_D = \frac{\text{output voltage}}{\text{input power}}$$

which characterizes the nonlinear element with its matching. If there is LO power delivered to the rectenna, the rectenna additionally acts as a mixing receiver.

As a first basic receiver module in SIMMWIC technology, we have investigated different rectenna circuits for the millimeter-wave range. The nonlinear rectifying element in the rectennas is a Schottky barrier diode integrated monolithically together with different antenna structures. A typical impedance curve of a Schottky diode over the frequency is shown in Fig. 1, together with the equivalent circuit. L_p and C_p are parasitic elements, R_s represents the series resistance of the diode, and R_j and C_j are the junction resistance and junction capacitance. From simulations and measurements (e.g., Fig. 8), they are found to be in the given range. The real part of the Schottky impedance lies around a few Ohms, at 5 Ω in this case, and is almost independent of frequency in the interesting frequency region. The imaginary part is capacitive with values of a few 10 Ω, and strongly dependent on frequency. To get maximum response to the incident RF power, the antenna impedance has to be matched to the diode impedance.

The layout of a monolithic slot-line rectenna is shown in Fig. 2. The rectifying element, a coplanar Schottky barrier diode, is integrated into the center of the slot-line antenna on high-resistivity silicon [2], [5]. In Fig. 3, the simulated

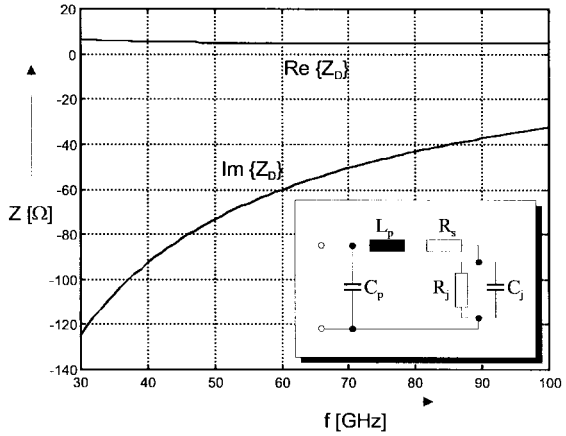


Fig. 1. Typical impedance curve of a Schottky diode over frequency. Inset: Schottky diode equivalent circuit ($R_j = 7$ kΩ, $C_j = 27$ fF, $R_s = 10\ \Omega$, $L_p = 20$ pH, $C_p = 15$ fF).

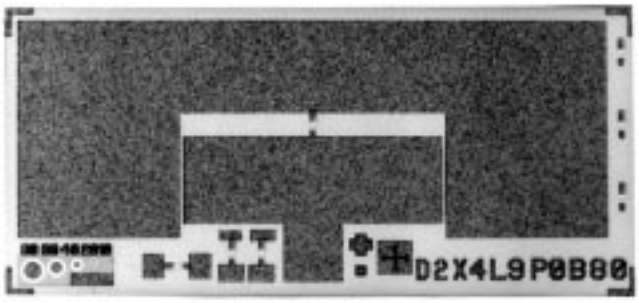


Fig. 2. Photo of the slot-line rectenna.

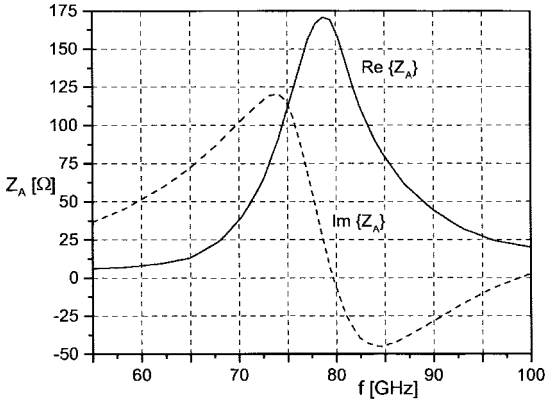


Fig. 3. Frequency-dependent impedance of the slot-line antenna.

impedance of a slot resonator at the locus of the Schottky diode is depicted. Comparing this impedance with the Schottky impedance shows that the matching condition $Z_A = Z_D^*$ is fulfilled around 60 GHz.

As a microstrip approach, two circuit layouts (shown in Fig. 4) were investigated. The first rectenna circuit provides a single Schottky barrier diode, whereas the second provides two diodes in series, which are also monolithically integrated on high-resistivity silicon. In the first case, the antenna part consists of 11 $\lambda/2$ elements arranged at half-wavelength distance along a microstrip line which conducts the millimeter-wave power to the Schottky diode. The diode is terminated

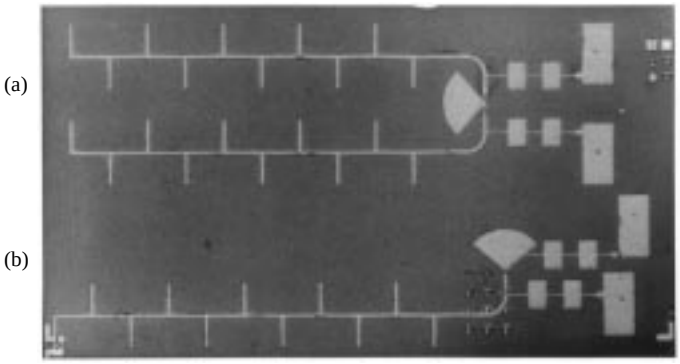


Fig. 4. Photo of the microstrip rectenna. (a) Two branches antenna with two Schottky diodes in series. (b) Antenna with single diode.

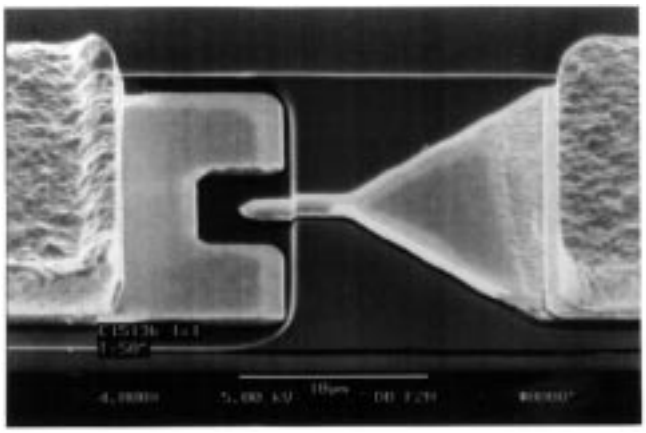


Fig. 5. SEM of a coplanar Schottky barrier diode.

by a radial-line sector. The second antenna consists of 20 receiving elements in a two-branch arrangement. The two diodes are terminated by a common radial-line sector. Two lines with filter structures are provided for biasing the Schottky diode and delivering the detected signal.

As a first approach of the cointegration of RF and IF or signal-processing functionalities, a microstrip rectenna with a CMOS preamplifier was combined as a two-chip module. The RF/CMOS multichip module (MCM) is mounted in a 24-lead dual in-line package (DIP) ceramic package [6].

III. Technical Realization

A. Fabrication Process for Integrated Schottky Diodes From Molecular Beam Epitaxy (MBE) Layers

Schottky barrier diodes are efficient detector elements for millimeter waves. In order to use them monolithically integrated into a receiver or mixer chip, they have to be realized in coplanar form (see Fig. 5). For proper working of these diodes in the millimeter-wave region, the series resistance and capacitance should be as small as possible. The Q factor of diodes for mixer applications is the cutoff frequency $f_{\rm co}$ given by

$$f_{\rm co} = 1/2\pi R_s C_j$$

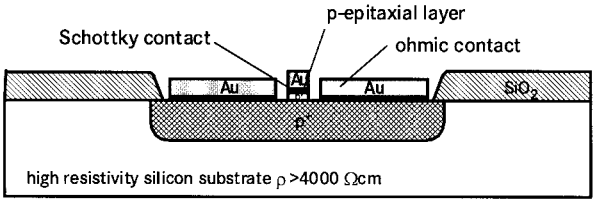


Fig. 6. Cross section of a coplanar p-Schottky barrier diode.

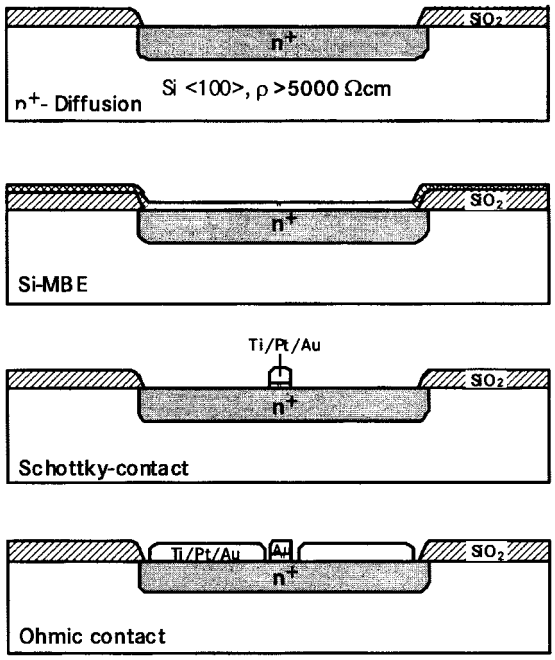


Fig. 7. Fabrication process for an n-Schottky barrier diode.

where R_s is the series resistance and C_j is the junction capacitance at 0 V.

To achieve the best mixer characteristics, the cutoff frequency should be ten times the detecting frequency. Junction capacitance is related to diode area, doping of epitaxial layer, and diffusion voltage (barrier height). Series resistance is also related to diode area and doping of epitaxial layer, but in the opposite sense. Therefore, an optimization of geometrical parameters (small area and minimal parasitic components) and doping parameters has to be performed to achieve a high cutoff frequency [7], [8].

The fabrication process of the diodes is described in detail in [9]. Both p- and n-diodes can be fabricated by the same mask set. Only the layer sequence in the fabrication process has to be changed for n-diodes from n^+-n to p^+-p (see Fig. 6) for p-diodes.

In the following, the fabrication process of n-diodes is described (see Fig. 7). As base material, high-resistivity silicon substrates are used: $(\rho > 5000\ \Omega \cdot \mathrm{cm})$. Using standard silicon technology processes, the substrates are first thermally oxidized and highly doped n^+ buried-layer regions are defined. This is done by As implantation (100 keV, $2 \cdot 10^{16}$ cm^{-2}) and subsequent diffusion at 1200 °C for 4 h. The resulting sheet resistance is 4.3 $\Omega/\square$ and a maximum As concentration at the surface of $1 \cdot 10^{20}$ cm^{-3} is achieved. The low sheet resistance and high surface concentration lowers series resistance and contact resistance of the diode. The n-epitaxial layer was grown by silicon MBE (Si-MBE). MBE offers low growth temperature, interface abruptness, and precise control of doping profile and thickness with nanometer resolution. A 80–100-nm-thick lightly doped semiconductor n-layer is grown by Si-MBE. The growth temperature was 550 °C. For the design of the millimeter-wave Schottky barrier diodes, the effect of the voltage-dependent depletion layer is taken into account. A complete depletion of the thin epitaxial layer is expected for doping levels up to $7 \cdot 10^{16}$ cm^{-3} (zero bias, 0.5-V Schottky barrier height). Both types of diodes (Schottky type with partially undepleted layer, Mott type with depleted layer at zero bias) have been realized. In some cases, Schottky barrier lowering was also achieved by an additional subsurface doping spike (10 nm, $2 \cdot 10^{18}$ Sb/cm^3 for n^+ doping spike, 10 nm $2 \cdot 10^{18}$ Ga/cm^3 for p^+ spike). These diodes may be operated under zero-bias conditions.

A differential growth technique is used where the epitaxial layer grows monocrystalline on silicon in the buried layer region and polycrystalline on the surrounding oxide [10]. The low-doped polycrystalline epitaxial layer is insulating and is used as an isolating layer for leading the Schottky anode finger from the active area to the outer oxide region.

The Schottky anode contact is formed by photolithographic patterning and a liftoff process with 50-nm Ti, 50-nm Pt, and 200-nm Au. The epitaxial layer is then plasma etched using the Schottky contact as an etch mask. The epitaxial layer is removed all over the wafer, except underneath the Schottky contact. Thus, access to the n^+ buried layer (ohmic contact) is achieved. The ohmic contact is formed using a second liftoff process with Ti, Pt, and Au metallization. The diodes are then passivated with a low-temperature plasma-enhanced chemical-vapor deposition (PECVD) silicon nitride. After opening contact windows to the Schottky and ohmic metallization layers, the rectenna metallization is defined and electroplated with gold to a thickness of 4 μm. Photos of the fabricated rectennas are depicted in Figs. 2 and 4.

B. DC- and RF-Characterization of the Planar Silicon Schottky Barrier Diodes

DC characteristics of the diodes are evaluated from *I–V* and CV measurements. Series resistance Rs, barrier height Φ, ideality factor n, and junction capacitance Cj strongly depend on doping parameters, diode geometry, and anode metallization. For n-diodes with titanium as Schottky anode metal, a barrier height of 0.5 V is determined from the saturation current, which corresponds to the theoretical value [12]. Series resistance is determined from the forward *I–V* characteristic at high currents (10 mA). The main contribution is due to the resistance of the epitaxial layer, which is fully undepleted at high currents. Fig. 8 shows measured series resistance values for different Schottky anode areas of two different wafers. The measured values correspond to an epitaxial layer thickness of 70 nm and a doping concentration of $2 \cdot 10^{16}$ cm^{-3}. Due to the low doping, the epitaxial layers are fully depleted up to an operation voltage of 0.25 V (Mott

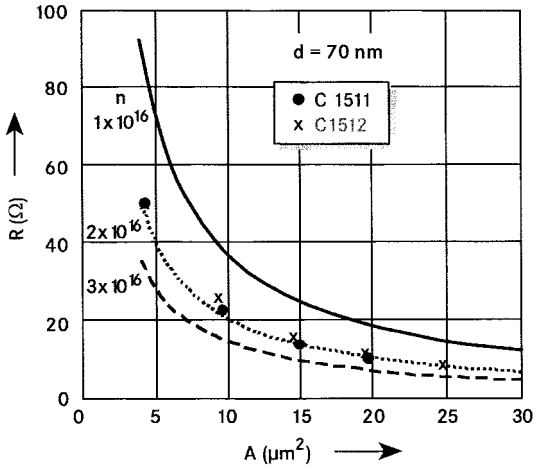


Fig. 8. Measured series resistance R of coplanar n -Schottky-barrier diodes for different anode areas A, and simulated resistance of the epitaxial layer for thickness $d = 70$ nm.

diode). Below this voltage, the resistance of the epitaxial layer does not contribute to the series resistance. Above 0.317 V, the epitaxial layer is fully undepleted and contributes to the series resistance.

CV measurements on mesa diodes yield a depletion width of 70 nm. This corresponds to a junction capacitance at zero volt of 1.5 fF/μm^2. Cutoff frequencies for p-type diodes up to 380 GHz and for n-type diodes up to 1 THz are achieved.

The diodes have also been characterized by measuring the scattering parameters in the frequency range from 1 to 60 GHz [14], [15]. Measured and simulated results fitted to an equivalent circuit model for n-Schottky barrier diodes are shown in the inset of Fig. 1. Fitting parameters for p-Schottky barrier diodes are given in [15].

n-Schottky-barrier diodes with a Schottky anode area of 12 μm^2 are mounted upside down in a single-ended mixer and tested at 94 GHz. With an LO power of 1 mW, a conversion loss of 10 dB is measured, with an LO power of 10 mW, a conversion loss of 6.5 dB is found. No bias is applied to the diodes (zero-bias operation). These values are comparable with results of planar and whisker contacted III–V mixers [13].

These n-type silicon Schottky diodes have also been used for the realization of a low-noise heterodyne 89-GHz monolithic microwave integrate circuit (MMIC) module for the multifrequency imaging microwave radiometer (MIMR) [16].

With p-type diodes, monolithic integrated single-balanced coplanar millimeter-wave mixers are realized in SIMMWIC technology. Barrier-height-reduced p-type Schottky diodes are used as mixing elements. At 77 GHz, a conversion loss of 7.8 dB is measured with an RF power of -10 dBm, an LO power of 6 dBm, and an IF of 1 GHz [15].

IV. Integration of CMOS With SIMMWIC

SIMMWIC and CMOS, both as silicon-based technologies, offer the potential of integrated solutions for millimeter-wave transmitter/receiver units with low-frequency signal readout. Technically speaking, this means CMOS circuits on high-resistivity silicon, a viable integration scheme for CMOS and millimeter-wave devices, and an economically meaningful fabrication sequence. Usual CMOS circuits are fabricated on moderately doped substrates or even on epitaxial layers on highly doped substrates. Both substrates are unacceptable for SIMMWIC's because of absorption of microwave radiation in conductive substrates. In principle, the CMOS process may be transferred to the necessary high-resistivity substrates when a few effects are considered and countermeasures are undertaken. The main effects to be considered are as follows.

1) Threshold voltage shift $\Delta V_{\rm th}$ by a different bulk doping

$$\Delta V_{\rm th} = -2\Delta\Psi_B - \frac{\Delta Q_B}{C_{\rm ox}} \tag{1}$$

where $\Psi_B = \Phi_F - \Phi_i$ is the difference between Fermi level Φ_F and intrinsic level Φ_i:

$$\Psi_B = \pm U_T \ln\frac{N}{ni}. \tag{2}$$

(U_T thermal voltage =26 meV at $T = 300$ K, N doping, n_i intrinsic carries density, $\pm$ for p- and n-channel, respectively.) The bulk-space charge Q_B is given by

$$Q_B \cdot C_{\rm ox} = \pm(4\varepsilon e N\Psi_B)^{1/2}. \tag{3}$$

($C_{\rm ox}$ oxide capacity $= \varepsilon_{\rm ox}/d_{\rm ox}$). Low doping generally shifts the behavior of the MOS transistor from enhancement type toward depletion type.

2) Low doping increases the space–charge width. Between source and drain, punchthrough of space–charge layers leads to pronounced short channel effects with enhanced subthreshold currents. This was experimentally confirmed with MOS transistors directly fabricated in high-resistivity silicon [4].

3) High-resistivity silicon is made by an FZ process (FZ silicon). Usually, the wafers for CMOS circuits are cut from Czochralski grown crystals (CZ silicon), which contains higher dopant and oxygen levels. Oxygen clusters are internally gettering metallic impurities. FZ silicon may contain, even with the same device processing, different levels of metallic impurities compared to CZ silicon and may, therefore, differ in the carrier lifetime properties. From the foregoing, it is clear that the MOS transistors should not be fabricated directly in the low-doped silicon substrate. Instead, a higher doped surface region would deliver straightforward solutions to the above-mentioned effects and problems. In a twin-tub solution [4], a conventional n-well hosts the P-metal–oxide semiconductor (PMOS) and a p-well in the p-substrate provides the required doping level for the n-metal–oxide–semiconductor (nMOS). In a surface-layer solution, the surface within the CMOS area is moderately n-doped, allowing CMOS fabrication as in an n-type substrate. The n-type surface layer has to be deep enough that punchthrough between the nMOS p-well and p-substrate is avoided. For a rapid assessment, we assume an exponential decay of the surface layer doping N_D with $N_D = N_W$ (p-well doping) at $Z = Z_W$ (p-well depth) and $N_D = N_S$ (substrate doping) at $Z = Z_S$ (substrate/surface layer interface). The punchthrough

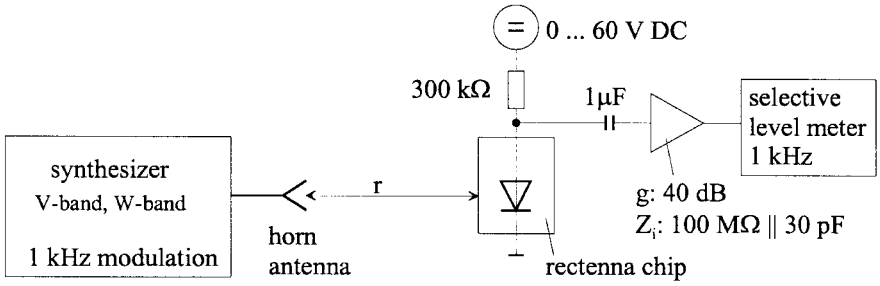


Fig. 9. Schematic drawing of the measuring setup for the rectenna.

voltage V_P and the extension of the n-surface layer beyond the p-well $(Z_S - Z_W)$ are connected by the following equation, which is obtained by integrating the Poisson equation:

$$\frac{\varepsilon[\ln(N_W/N_S)]^2}{eN_W}\cdot\frac{V_i+V_P}{(Z_W-Z_S)2}=1-\frac{N_S}{N_W}\left[1+\ln\left(\frac{N_W}{N_S}\right)\right] \tag{4}$$

V_i built-in voltage of the p-well/n-layer junction.

The right-hand side of (4) approaches unity for realistic values $N_S/N_W \ll 1$. For a required punchthrough voltage V_P and given p-well data (N_W, Z_W), this equation shows how deep (Z_S) the n-surface layer should be.

A hybrid integration of a CMOS preamplifier and a 90-GHz rectenna in an MCM is reported in the Section V. The carrier for the MCM was also made from high-resistivity silicon to avoid microwave absorption.

For monolithic integration, we propose the following integration scheme. In a first step, the CMOS circuit is fabricated without the final Al metallization step. Then, in the SIMMWIC area, the vertical epitaxy structure is deposited, laterally defined, and contacted. As a last step, in the wafer process, the metallization and the passivation for CMOS and SIMMWIC is performed. The scheme is only economically meaningful if a common metallization system (Al, Cu) is used. Now, mainly Au-based metallization systems are used for millimeter-wave circuits. An investigation of the influence of Al metallization on SIMMWIC properties was started, and results of this investigation will be reported later.

V. Results

For measuring the rectenna sensitivity, a computer-controlled measurement setup (shown in Fig. 9) with a V- or W-band sweeper and a waveguide horn antenna as the radiation source was used. The millimeter-wave signal was modulated with 1 kHz to separate the received signal and the bias voltage. After amplification with a high-input impedance amplifier, the rectenna signal was measured with a frequency selective level meter at 1 kHz. The rectenna chips were placed at a distance r in the far-field main beam of the horn with respect to the polarization. With the gain of the horn antenna and the distance, the power density at the locus of the rectenna was calculated.

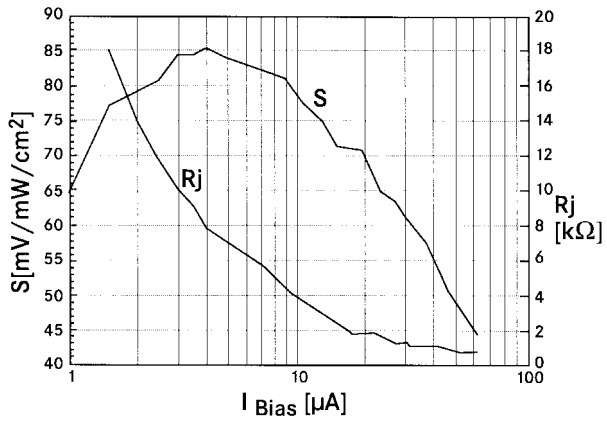
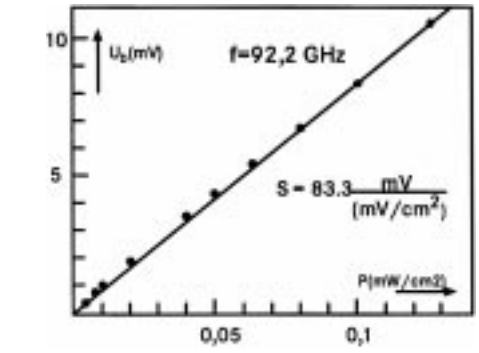


Fig. 10. Sensitivity of the slot-line rectenna and junction resistance versus bias current.

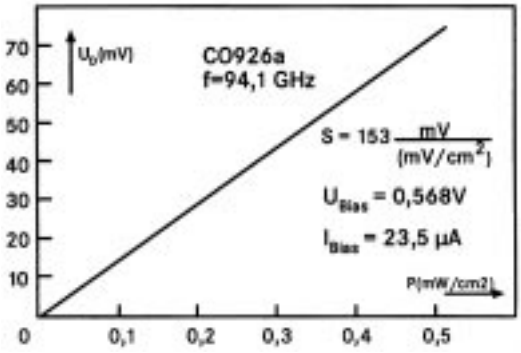
Fig. 10 shows the measured sensitivity of the slot-line rectenna with a 0.9-mm slot as a function of the Schottky bias current. The bias dependence of the junction resistance is also depicted in Fig. 10. The maximum sensitivity measured is 85.3 mV/mW/cm^2 at a bias current of 4 μA. The signal frequency was 63.6 GHz.

In Fig. 11, the measured sensitivities of the microstrip rectennas are shown. With the one-branch type, a sensitivity of 83.3 mV/mW/cm^2 at 92.2 GHz was reached with a zero bias p-Schottky barrier diode. The radiation pattern of this circuit is depicted in Fig. 12. The two-branch antenna type gives a sensitivity of 153 mV/mW/cm^2 with 23.5 μA bias at 94.1 GHz [see Fig. 11(b)].

For the RF/CMOS MCM, a standard single-inverter stage CMOS preamplifier with 32-dB gain operated with supply voltages of $\pm$6 V was employed. Amplifiers with differential inputs and two stages offering low-frequency gains of around 70 dB have also been realized on standard CMOS substrates (CZ, n-type, 4–6 $\Omega\cdot$cm, $\langle 100\rangle$ oriented) and on high-resistivity substrates (FZ, p-type, 5000–7000 $\Omega\cdot$ cm, $\langle 100\rangle$). The FZ substrate material is required to keep RF substrate losses low in the case of future monolithic integration of SIMMWIC RF circuits with analog- and digital-circuit functions realized in CMOS technology. A comparison of these amplifiers and single MOS devices fabricated on both substrate materials showed a good similarity in electrical behavior and a preservation of the high-resistivity substrate characteristics outside the CMOS region.



(a)



(b)

Fig. 11. Output voltage of the rectenna versus RF power density for (a) the one-branch type with $I_{\mathrm{Bias}} = 0$ V and (b) the two-branch type of Fig. 2 with $I_{\mathrm{Bias}} = 23.5$ μA.

Problems to be kept in mind regarding CMOS on FZ substrates are increased leakage due to lower substrate doping, facilitated punchthrough effects, and the nonexistence of internal gettering as exhibited by CZ substrates. An alternative solution to these problems may be the usage of silicon-on-isolator (SOI) substrates on high-resistivity silicon [17]. SOI substrates prevent leakage current, minimize parasitic capacitance, allow good isolation of the active devices, and improve the overall speed of the CMOS circuits [18]. So far, the results offer a good prospect for monolithically integrated SIMMWIC/CMOS circuits in the near future.

The single-inverter-stage CMOS preamplifier was chosen because of low-offset voltage and better temperature stability. The amplifier operates with a symmetrical dc supply of ± 6 V and has a low offset voltage of 12 mV. The low-frequency gain is 32 dB. The detector chip is combined with the CMOS preamplifier as an MCM in a hybrid construction. This was done as an early stage of the combination of SIMMWIC technology with standard CMOS technology. Likewise, the monolithic integration is not possible or useful in every case. The high-frequency chip for millimeter-wave detection and the low-frequency chip for amplification are mounted on a common substrate material—a silicon substrate (see Fig. 13). This hybrid technology offers some advantages over monolithic integration, e.g., different technologies for the monolithic integration can be used, different backside processing of the different chips is possible, and there is a free choice of substrate potential for the single chips. Either conductive or nonconductive adhesive is possible.

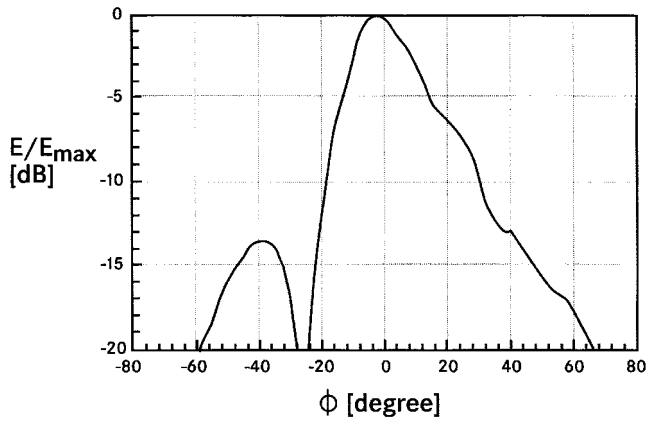


Fig. 12. H-plane radiation pattern at 92.2 GHz of the one-branch microstrip rectenna.

The SIMMWIC chip is mechanically thinned to a thickness of 100 μm due to the microstrip design of the antenna while the CMOS chip remains unthinned. As mechanical carrier a 7.5 $\times$ 20 mm^2 sized piece of an unthinned silicon wafer ($\langle 111 \rangle$-oriented, high-resistivity material with a thickness of 280 μm) is used. The silicon substrate material is thermally oxidized to a thickness of 1 μm to avoid a conductive connection between the substrates of the CMOS and SIMMWIC chip. In this case, a conductive adhesive layer is used, but there is no problem in using a nonconductive adhesive. The signal connection is realized by one aluminum bond wire connecting the output of the rectenna to the input of the amplifier (see Fig. 13). The amplifier needs no special ground connection, thus no further connection to the rectenna is needed. The RF/CMOS MCM is mounted in a 24-lead DIP ceramic package (see Fig. 13).

Fig. 14 depicts the measured output signal as a function of the RF power density at a frequency of 94.6 GHz. The sensitivity of the configuration is 1600 mV/mW/cm^2, including the 32-dB amplifier gain. The frequency response is depicted in Fig. 15 and the radiation pattern in Fig. 16, which shows a 3-dB bandwidth of 1.6 GHz.

VI. Discussion

Due to the low-substrate costs, SIMMWIC technology enables the cost-effective monolithic integration of antennas, passive networks, and active devices into single-chip microsystems. Thus, complete transmitter and receiver circuits can be realized on one single chip. This is demonstrated with the presented SIMMWIC rectenna chips and with active SIMMWIC antennas [2]. Many new single-chip RF microsystems are expected with the further development of the Si/SiGe HBT in the near future.

A next step will be the cointegration of RF circuitry with standard CMOS signal-processing circuits. This was demonstrated with a hybrid combination of an RF circuit with a CMOS preamplifier as an early stage of combination of SIMMWIC technology with standard CMOS technology. The fabrication of CMOS circuits on high-resistivity silicon substrates is promising and should allow the cointegration of SIMMWIC's with CMOS signal-processing circuits in the near future.

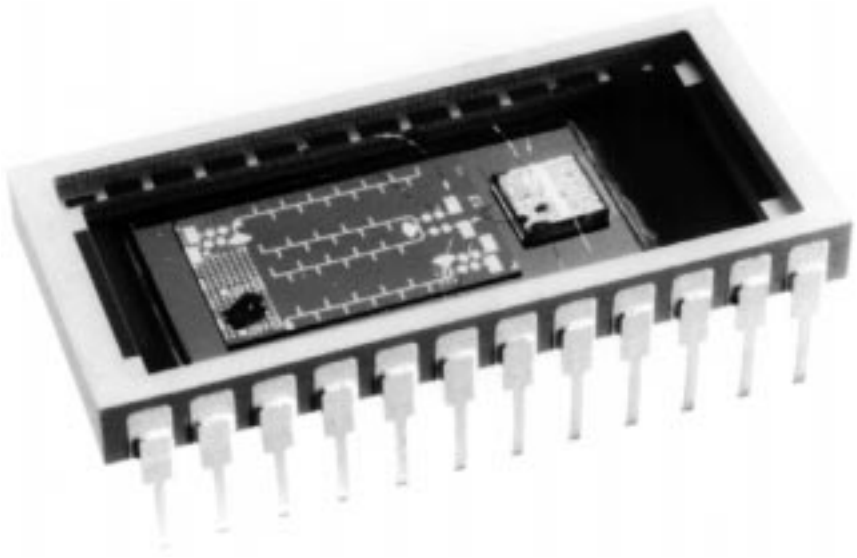


Fig. 13. Photo of the RF/CMOS MCM.

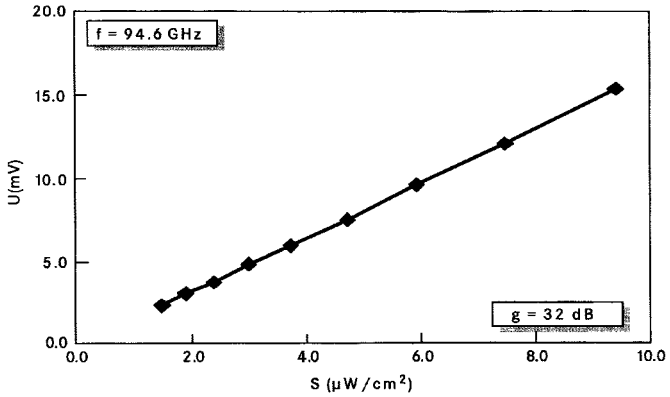


Fig. 14. Output voltage of the rectenna/CMOS MCM versus RF power density.

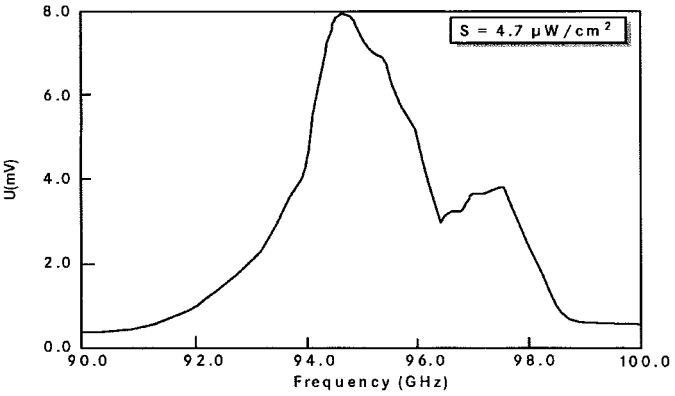


Fig. 15. Output voltage of the rectenna/CMOS MCM versus frequency ($S = 4.7\ \mu\mathrm{W/cm^2}$).

With a suitable mounting of the receiver chips, they can be operated as field detectors and as field-coupled LO mixing receivers, respectively. In a future receiver scenario, one could imagine a single-SIMMWIC-chip solution with a switched antenna with variable beam characteristics and a preamplifier.

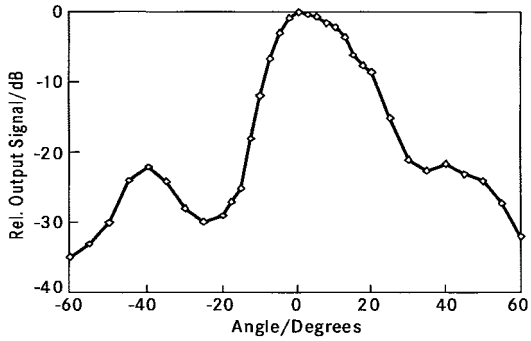


Fig. 16. *H*-plane radiation pattern of the packaged rectenna/CMOS module.

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